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EXAMINER
TECKLU, ISAAC TUKU

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 01/04/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,558	07/01/2003	Daniel V. Zilavy	200208005-1	2291

TITLE OF INVENTION: FIELD-REPLACEABLE UNIT REVISION COMPATIBILITY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/05/2010

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT.
PROSECUTION ON THE MERITS IS CLOSED.   THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS.
THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON
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**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE
MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED.   THIS
STATUTORY PERIOD CANNOT BE EXTENDED.   SEE 35 U.S.C. 151.   THE ISSUE FEE DUE INDICATED ABOVE DOES
NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION.   IF AN ISSUE FEE HAS
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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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_____ (Depositor's name)

_____ (Signature)

_____ (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,558	07/01/2003	Daniel V. Zilavy	200208005-1	2291

TITLE OF INVENTION: FIELD-REPLACEABLE UNIT REVISION COMPATIBILITY

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nonprovisional	NO	$1510	$300	$0	$1810	04/05/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
TECKLU, ISAAC TUKU	2192	717-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

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1 _____

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE   (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) :   ☐ Individual   ☐ Corporation or other private group entity   ☐ Government

4a. The following fee(s) are submitted:

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☐ Publication Fee (No small entity discount permitted)

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4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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EXAMINER
TECKLU, ISAAC TUKU

ART UNIT	PAPER NUMBER
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DATE MAILED: 01/04/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 842 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 842 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

	Application No.	**Applicant(s)**
Notice of Allowability	10/611,558	ZILAVY, DANIEL V.
	Examiner	**Art Unit**
	ISAAC T. TECKLU	2192

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to <u>09/22/2009</u>.

2. ☒ The allowed claim(s) is/are <u>1, 5-12, 16-18, 23-24, 28-29, 42-45, 49-52, 56-57, 61-62, and 66 (renumbered as 1-30)</u>.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All   b) ☐ Some*   c) ☐ None   of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

     * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

    Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>12/08/09</u>

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application

6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☒ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192

DETAILED ACTION

1.   This action is responsive the application filed on 09/22/2009.

2.   Claims 2-4, 13-15, 19-21, 25-27, 30-41, 46-48, 53-55, 58-60, and 63-65 have been cancelled.

3.   Claims 1, 5-12, 16-18, 22-24, 28-29, 42-45, 49-52, 56-57, 61-62, and 66 are allowed.

EXAMINER'S AMENDMENT

4.   An examiner's amendment to the record appear below. Should the change and/or additions be unacceptable to the Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such amendment, it MUST be submitted no later than the payment of issue fee.

Authorization for examiner's amendment was given in a telephone interview with Robert W. Nelson, Reg. No. 37,898, on July 17, 2009 to put the case in condition for allowance. The application has been amended as follows:

IN THE CLAIMS:

Please cancel claims 2-4, 13-15, 19-21, 25-27, 46-48, 53-55, 58-60, and 63-65 and amend claims 1, 5, 12, 16, 18, 22, 24, 28, 42, 45, 49, 52, 56, 57, 61, 62, and 66 as follows:

1. (Currently Amended) In a computer system including a first field-programmable unit including first field-programmable unit (FPU) of a first type, the first FPU including first field-programmable code, a second FPU of a second type including a second FPU code, a plurality of field-programmable units including a corresponding plurality of FPU codes, a computer-implemented method comprising steps of:

(A) determining whether the first FPU and the first FPU code are compatible with the second FPU and second FPU code; [[and]]-

(B) if the first FPU and the first FPU code are determined not to be compatible with the second FPU and second FPU code, notifying a user of the computer system of the incompatibility, wherein the step (A) comprises a step of:

(A)(1) determining whether the first FPU code is compatible with at least one of the plurality of FPU codes, wherein the computer system further comprises a plurality of field-replaceable units, and wherein the step (A) further comprises a step of:

(A)(2) determining whether the first FPU code is compatible with the plurality of field-replaceable units, wherein the computer system further comprises a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the step (A)(1) comprises a step of determining that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of field-programmable unit codes identified by the revision compatibility descriptor.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The method of claim [[2]] 1, wherein the computer system further comprises a plurality of field-replaceable units and a revision compatibility descriptor identifying a

plurality of compatible combinations of field-programmable unit codes and field-replaceable units,

and wherein the step (A) comprises a step of determining that the first FPU code is compatible with

the computer system if a combination of the first FPU code, the plurality of FPU codes, and the

plurality of field-replaceable units is among the plurality of combination combinations of field-

programmable unit codes and field-replaceable units identified by the revision compatibility

descriptor.

12. (Currently Amended) In a computer system including a first field-programmable unit FPU of a

first type, the first FPU including first field-programmable unit code, a plurality of field-

programmable units including a corresponding plurality of FPU codes, a plurality of field-replaceable

units, an apparatus comprising:

        a processor;

        determination means for determining whether the first FPU and first FPU code

are compatible with a second FPU and second FPU code, wherein the second FPU

includes the second FPU code, and wherein the second FPU is of a second type that

differs from the first type, and wherein both the first FPU and the second FPU are

connected to the computer system; [[and]]

        notification means for notifying a user of the computer system that the first FPU

and first FPU code are not compatible with the second FPU and second FPU code if the

determination means determines that the first FPU and first FPU code are not

compatible with the second FPU and second FPU code, wherein the determination means

comprises:

means for determining whether the first FPU code is compatible with the plurality of FPU codes, wherein the determination means further comprises:

means for determining whether the first FPU code is compatible with the plurality of field-replaceable units, and

means for determining whether the first FPU code is compatible with the plurality of field-replaceable units, further comprising a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the determination means comprises means for determining that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of field-programmable unit codes identified by the revision compatibility descriptor.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The apparatus of claim [[13]] 12, wherein the computer system further comprises a plurality of field-replaceable units, wherein the apparatus further comprises a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes and field-replaceable units, and wherein the determination means comprises means for determining that the first FPU code is compatible with the computer system if a combination of the first FPU code, the plurality of FPU codes, and the plurality of field-

replaceable units is among the plurality of combination combinations of field-programmable unit codes and field-replaceable units identified by the revision compatibility descriptor.

18. (Currently Amended) A storage medium readable by a computer in a computer system including a first field-programmable unit of a first type, the first field-programmable unit including first field-programmable unit (FPU) code, a plurality of field-programmable units including a corresponding plurality of FPU codes, a plurality of field-replaceable units, the storage medium tangibly embodying program instructions executable by the computer to perform method steps of:

      (A) determining whether the first FPU and the first FPU code are compatible with a second FPU and second FPU code the computer system, wherein the second FPU includes the second FPU code, wherein the second FPU is of a second type that differs from the first type, and wherein both the first FPU and the second FPU are connected to the computer system; and

      (B) if the first FPU and first FPU code are determined not to be compatible with the second FPU and second FPU code, notifying a user of the computer system of the incompatibility, wherein the step (A) comprises a step of:

      (A)(1) determining whether the first FPU code is compatible with the plurality of FPU codes, wherein the step (A) further comprises a step of:

      (A)(2) determining whether the first FPU code is compatible with the plurality of field replaceable units, wherein the computer system further comprises a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the step (A)(1) comprises a step of determining that the first FPU code is compatible with the

plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is

among the plurality of compatible combinations of field-programmable unit codes identified by

the revision compatibility descriptor.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) The storage medium of claim [[19]] 18, wherein the computer system

further comprises a plurality of field-replaceable units and a revision compatibility descriptor

identifying a plurality of compatible combinations of field-programmable unit codes and

field-replaceable units, and wherein the step (A) comprises a step of determining that

the first FPU code is compatible with the computer system if a combination of the first

FPU code, the plurality of FPU codes, and the plurality of field-replaceable units is

among the plurality of combination combinations of field-programmable unit codes and

field-replaceable units identified by the revision compatibility descriptor.

24. (Currently Amended) A computer system comprising:

        a processor;

        a first field-programmable unit (FPU) of a first type, the first FPU including first

FPU code;

a second field-programmable unit (FPU) of a second type, the second FPU including second FPU code, wherein both the first FPU and the second FPU are connected to the computer system;

a compatibility verifier coupled to the first FPU and operable to determine whether the first FPU and the first FPU code are compatible with the second FPU and second FPU code the computer system, and to notify a user of the computer system of the incompatibility if the first FPU and first FPU code are determined not to be compatible with the second FPU and second FPU code.

a plurality of field- programmable units including a corresponding plurality of FPU codes, and wherein the compatibility verifier is further operable to determine whether the first FPU code is compatible with the plurality of FPU codes

a plurality of field-replaceable units, and wherein the compatibility verifier is further operable to determine whether the first FPU code is compatible with the plurality of field-replaceable units

a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the compatibility verifier is operable to determine that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of field-programmable unit codes identified by the revision compatibility descriptor.

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Currently Amended) The computer system of claim [[25]] 24, further comprising a plurality of field-replaceable units and a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes and field-replaceable units, and wherein the compatibility verifier is operable to determine that the first FPU code is compatible with the computer system if a combination of the first FPU code, the plurality of FPU codes, and the plurality of field-replaceable units is among the plurality of combination combinations of field-programmable unit codes and field-replaceable units identified by the revision compatibility descriptor.

42. (Currently Amended) A computer system comprising:

> a processor;

> a first field-programmable unit (FPU) comprising first FPU code;

> a second FPU comprising second FPU code; [[and]]

> a compatibility verifier coupled to the first FPU, the compatibility verifier being operable to determine whether the first FPU code is different from the second FPU code and, if the first FPU code is determined to be different from the second FPU code, to notify a user of the computer system that the first FPU code is incompatible with the computer system,

> a plurality of field- programmable units including a corresponding plurality of FPU codes, and wherein the compatibility verifier is further operable to determine whether the first FPU code is compatible with the plurality of FPU codes,

a plurality of field-replaceable units, and wherein the compatibility verifier is further operable to determine whether the first FPU code is compatible with the plurality of field-replaceable units,

a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the compatibility verifier is operable to determine that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of field-programmable unit codes identified by the revision compatibility descriptor.

45. (Currently Amended) In a computer system including a first field-programmable unit (FPU) of a first type, the first FPU including first FPU code, a plurality of field-programmable units including a corresponding plurality of FPU codes, a plurality of field-replaceable units a computer-implemented method comprising steps of:

(A) determining whether the first FPU and first FPU code are compatible with a second FPU and second FPU code wherein both the first FPU and the second FPU are in the computer system, wherein the second FPU includes the second FPU code, and wherein the second FPU is of a second type that differs from the first type;

(B) if the first FPU and first FPU code are determined not to be compatible with the second FPU and second FPU code, identifying third FPU code that is compatible with the computer system and suitable for installation in the first field-programmable unit; and

(C) installing the third FPU code in the first field-programmable unit, and wherein the step (A) comprises a step of:

(A)(1) determining whether the first FPU code is compatible with the plurality of FPU codes,

wherein the step (A) further comprises a step of:

(A)(2) determining whether the first FPU code is compatible with the plurality of field-replaceable units, wherein the computer system further comprises a revision compatibility descriptor identifying a plurality of compatible combinations of FPU codes, and wherein the step (A)(1) comprises a step of determining that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of FPU identified by the revision compatibility descriptor.

46. (Cancelled)

47. (Cancelled)

48. (Cancelled)

49. (Currently Amended) The method of claim [[46]] 45, wherein the computer system further comprises a plurality of field-replaceable units and a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes and field-replaceable units, and wherein the step (A) comprises a step of determining that the first FPU code is compatible with the computer system if a combination of the first FPU code, the plurality of FPU codes, and the plurality of field-replaceable units is among the plurality of combination combinations of FPU codes and field-replaceable units identified by the revision compatibility descriptor.

52. (Currently Amended) In a computer system including a first field-programmable

unit (FPU) of a first type, the first FPU including first FPU code, an apparatus

comprising:

    a processor;

    determination means for determining whether the first FPU and first FPU code

are compatible with a second FPU and second FPU code, wherein both the first FPU

and the second FPU are in the computer system, wherein the second FPU includes the

second FPU code, and wherein the second FPU is of a second type that differs from the

first type;

    identification means for identifying third FPU code that is compatible with the

computer system and suitable for installation in the first field-programmable unit if the

first FPU and first FPU code are determined not to be compatible with the second FPU

and second FPU code; [[and]]

    installation means for installing the third FPU code in the first field-programmable

unit, wherein the computer system further comprises a plurality of field-programmable units

including a corresponding plurality of FPU codes, and wherein the determination means comprises:

    means for determining whether the first FPU code is compatible with the plurality

of FPU codes, wherein the computer system further comprises a plurality of field-replaceable units,

and wherein the determination means further comprises:

means for determining whether the first FPU code is compatible with the plurality

of field-replaceable units, wherein the computer system further comprises a revision compatibility

descriptor identifying a plurality of compatible combinations of FPU codes, and wherein the

determination means comprises means for determining that the first FPU code is compatible with

the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is

among the plurality of compatible combinations of FPU identified by the revision compatibility

descriptor.

53. (Cancelled)

54. (Cancelled)

55. (Cancelled)

56. (Currently Amended) The apparatus of claim [[53]] 52, wherein the computer system further

comprises a plurality of field-replaceable units and a revision compatibility descriptor

identifying a plurality of compatible combinations of field-programmable unit codes and

field-replaceable units, and wherein the determination means comprises means for

determining that the first FPU code is compatible with the computer system if a

combination of the first FPU code, the plurality of FPU codes, and the plurality of field-

replaceable units is among the plurality of combination combinations of FPU codes and

field-replaceable units identified by the revision compatibility descriptor.

57. (Currently Amended) A storage medium readable by a computer in a computer system including

a first field-programmable unit (FPU) of a first type, the first FPU including first FPU code, a

plurality of field-programmable units including a corresponding plurality of FPU codes, a plurality of

<u>field replaceable units including a corresponding plurality of FPU codes,</u> the storage medium

tangibly embodying program instructions executable by the computer to perform method steps of:

(A) determining whether the first FPU and first FPU code are compatible with a

second FPU and second FPU, wherein both the first FPU and the second FPU are in

the computer system, wherein the second FPU includes the second FPU code, and

wherein the second FPU is of a second type that differs from the first type;

(B) if the first FPU code is determined not to be compatible with the computer

system, identifying third FPU code that is compatible with the computer system and

suitable for installation in the first field-programmable unit; and

(C) installing the third FPU code in the first field-programmable unit <u>wherein the step (A)</u>

<u>comprises a step of:</u>

<u>(A)(1) determining whether the first FPU code is compatible with the plurality of</u>

<u>FPU codes,</u>

<u>(A)(2) determining whether the first FPU code is compatible with the plurality of field-</u>

<u>replaceable units, wherein the computer system further comprises a revision compatibility descriptor</u>

<u>identifying a plurality of compatible combinations of FPU codes, and wherein the determination</u>

<u>means comprises means for determining that the first FPU code is compatible with the plurality of</u>

<u>FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the</u>

<u>plurality of compatible combinations of FPU identified by the revision compatibility descriptor.</u>

58. (Cancelled)

59. (Cancelled)

60. (Cancelled)

61. (Currently Amended) The storage medium of claim [[58]] 57, wherein the computer system

further comprises a plurality of field-replaceable units and a revision compatibility descriptor

identifying a plurality of compatible combinations of field-programmable unit codes and

field-replaceable units, and wherein the step (A) comprises a step of determining that

the first FPU code is compatible with the computer system if a combination of the first

FPU code, the plurality of FPU codes, and the plurality of field-replaceable units is

among the plurality of combination combinations of FPU codes and field-replaceable

units identified by the revision compatibility descriptor.

62. (Currently Amended) A computer system comprising:

       a processor;

       a first field-programmable unit (FPU) of a first type, the first FPU including first

FPU code;

       a compatibility verifier coupled to the first FPU and operable to determine whether the first

FPU and first FPU code are compatible with a second FPU and second FPU code, wherein both the

first FPU and the second FPU are connected to the computer system, and, if the first FPU and first

FPU code are determined not to be compatible with the second FPU and second FPU code, to

identify third FPU code that is compatible with the computer system and suitable for installation in

the first field-programmable unit; [[and]]

a code installer coupled to the first FPU and operable to install the third FPU code in the

first field-programmable unit, further comprising a plurality of FPUs including a corresponding

plurality of FPU codes, and wherein the compatibility verifier is operable to determine whether the

first FPU code is compatible with the plurality of FPU codes, further comprising a plurality of field-

replaceable units, and wherein the compatibility verifier is operable to determine whether the first

FPU code is compatible with the plurality of field-replaceable units, further comprising a revision

compatibility descriptor identifying a plurality of compatible combinations of FPU codes, and

wherein the compatibility verifier is operable to determine that the first FPU code is

compatible with the plurality of FPU codes if a combination of the first FPU code and the

plurality of FPU codes is among the plurality of compatible combinations of FPU

identified by the revision compatibility descriptor.

63. (Original)

64. (Original)

65. (Original)

66. (Currently Amended) The computer system of claim [[63]] 62, further comprising a plurality of

field-replaceable units and a revision compatibility descriptor identifying a plurality of compatible

combinations of field-programmable unit codes and field-replaceable units, and wherein the

compatibility verifier is operable to determine that the first FPU code is compatible with the

computer system if a combination of the first FPU code, the plurality of FPU codes, and the

plurality of field-replaceable units is among the plurality of combination combinations of FPU codes

and field-replaceable units identified by the revision compatibility descriptor.

--End--

Allowable Subject Matter

5.   The following is an examiner's statement of reasons for allowance:

As applicant pointed out under Remark section, pages 10-13, Sprecher et al. (US 6,948,059 B1), taken either singly and/or in combination with other cited prior arts, do not teach the combined functional limitations of (A)(1) determining whether the first FPU code is compatible with at least one of the plurality of FPU codes, wherein the computer system further comprises a plurality of field-replaceable units, and wherein the step (A) further comprises a step of: (A)(2) determining whether the first FPU code is compatible with the plurality of field-replaceable units, wherein the computer system further comprises a revision compatibility descriptor identifying a plurality of compatible combinations of field-programmable unit codes, and wherein the step (A)(1) comprises a step of determining that the first FPU code is compatible with the plurality of FPU codes if a combination of the first FPU code and the plurality of FPU codes is among the plurality of compatible combinations of field-programmable unit codes identified by the revision compatibility descriptor, as recited in such manners in each of independent claims 1, 12, 18, 24, 42, 45, 52, 57, and 62.

Prior arts of record do not teach and/or suggest these claimed limitations, thus, all remaining pending claims 1, 5-12, 16-18, 22-24, 28-29, 42-45, 49-52, 56-57, 61-62, and 66 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6.   Any inquiry concerning this communication or earlier communications from the examiner

should be directed to ISAAC T. TECKLU whose telephone number is (571) 272-7957. The

examiner can normally be reached on M-TH 9:300A - 8:00P.

       If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization

where this application or proceeding is assigned is 571-273-8300.

       Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system,

see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system,

contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like

assistance from a USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Isaac T Tecklu/   /Tuan Q. Dam/
Examiner, Art Unit 2192   Supervisory Patent Examiner, Art Unit 2192